AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (PREVIOUSLY AMENDED) A spread spectrum clock generator circuit comprising:

a first circuit configured to generate a clock signal in response to (i) a reference signal, (ii) a sequence of spread spectrum ROM codes, and (iii) a command signal, wherein (i) said clock signal is spread spectrum modulated and (ii) said spread spectrum modulation of said clock signal can be switched on and off in response to said command signal; and

a second circuit configured to synchronize said command signal to a feedback signal, wherein said sequence of spread spectrum ROM codes is generated according to a predetermined mathematical formula and optimized in accordance with predetermined criteria.

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4. (PREVIOUSLY AMENDED) The spread spectrum clock generator circuit according to claim 1, wherein said spread spectrum clock generator circuit is used with a motherboard or CPU.

5. (PREVIOUSLY AMENDED) The spread spectrum clock generator circuit according to claim 1, wherein said second circuit is further configured to generate one or more control signals in response to (i) said command signal and (ii) said feedback signal.

6. (PREVIOUSLY AMENDED) The spread spectrum clock generator circuit according to claim 5, wherein said second circuit comprises a first latch.

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7. (PREVIOUSLY AMENDED) The spread spectrum clock generator circuit according to claim 6, wherein said second circuit further comprises a second latch.

8. (PREVIOUSLY AMENDED) The spread spectrum clock generator circuit according to claim 1, wherein said predetermined criteria are applied to said clock signal during a transition period when spread spectrum modulation is switching on or switching off.

9. (PREVIOUSLY AMENDED) The spread spectrum clock generator circuit according to claim 1, wherein said predetermined criteria includes a predetermined minimum frequency for said clock signal.

10. (PREVIOUSLY AMENDED) The spread spectrum clock generator circuit according to claim 7, wherein said predetermined criteria further includes a predetermined maximum frequency for said clock signal.

11. (CURRENTLY AMENDED) The spread spectrum clock generator circuit according to claim 1, wherein said predetermined mathematical formula is:

$$\begin{bmatrix} X1(N+1) \\ X2(N+1) \\ X3(N+1) \end{bmatrix} = \begin{bmatrix} 0 & -\frac{VCO}{FBD(N+1)} & 0 \\ \frac{CP(N+1)}{C1} & -\frac{1}{C1 \cdot R1} & -\frac{1}{C1 \cdot R1} \\ 0 & \frac{1}{C2 \cdot R1} & -\frac{1}{C2 \cdot R1} \end{bmatrix} \begin{bmatrix} X1(N) \\ X2(N) \\ X3(N) \end{bmatrix} * \Delta t(N) + \begin{bmatrix} U1(N+1) \\ U2(N+1) \\ U3(N+1) \end{bmatrix} * \Delta t(N) + \begin{bmatrix} X1(N) \\ X2(N) \\ X3(N) \end{bmatrix}$$

where X represents a value of said clock signal, VCO represents a voltage controlled oscillator gain, C1 and C2 represent capacitance values, R1 represents a resistance value, FBD represents a feedback divider value, $\Delta t(N)$ represents a time interval between a last time step and a present time, U represents said reference signal, CP represents a charge pump current and N represents a time step.

12. (PREVIOUSLY AMENDED) The spread spectrum clock generator circuit according to claim 1, wherein:

said sequence of spread spectrum ROM codes is optimized using a computer program to simulate transient behavior.

13. (PREVIOUSLY AMENDED) A spread spectrum clock generator circuit comprising:

means for generating a clock signal in response to (i) a reference signal, (ii) a sequence of spread spectrum ROM codes and (iii) a command signal, wherein (i) said clock signal is spread spectrum modulated and (ii) said spread spectrum modulation of said clock signal can be switched on and off in response to said command signal; and

means for synchronizing said command signal to a feedback signal, wherein said sequence of spread spectrum ROM codes is generated according to a predetermined mathematical formula and optimized in accordance with predetermined criteria.

14. (PREVIOUSLY AMENDED) A method for controlling a spread spectrum transition comprising the steps of:

generating a clock signal in response to (i) a reference signal, (ii) a sequence of spread spectrum ROM codes and (iii) a command signal, wherein said clock signal is spread spectrum modulated and (ii) said spread spectrum modulation of said clock signal can be switched on and off in response to said command signal; and

synchronizing said command signal to a feedback signal, wherein said sequence of spread spectrum ROM codes is generated

according to a predetermined mathematical formula and optimized in accordance with predetermined criteria.

15. (ORIGINAL) The method according to claim 14, wherein the step of generating said sequence of spread spectrum ROM codes further comprises the sub-steps of:

(A) selecting a number of ROM codes to be used to generate a spread spectrum modulation signal; and

(B) generating said number of ROM codes according to said predetermined mathematical formula.

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16. (PREVIOUSLY AMENDED) The method according to claim 15, wherein the step of selecting said ROM codes further comprises the sub-steps of:

(A) initializing a phase lock loop (PLL) at power supply ramping;

(B) stabilizing said PLL with spread spectrum modulation turned off;

(C) loading said sequence of spread spectrum ROM codes;

(D) switching on spread spectrum modulation;

(E) recording transient behavior of said clock signal until PLL is in spread spectrum steady-state;

(F) switching off spread spectrum modulation;

(G) recording transient behavior of said clock signal until spread spectrum modulation is completely off;

(H) comparing recorded transient behavior to predetermined criteria;

(I) if the recorded transient behavior does not meet said predetermined criteria, shifting said sequence of spread spectrum ROM codes, wherein a last ROM code is moved to a first position and remaining ROM codes are shifted one position forward;

(J) if the recorded transient behavior meets said predetermined criteria, finalizing said sequence of spread spectrum ROM codes; and

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(K) repeating sub-steps (D) through (J) until said recorded transient response meets said predetermined criteria.

17. (ORIGINAL) The method according to claim 16, wherein said sub-steps are performed by a computer program.

18. (ORIGINAL) The method according to claim 14, wherein said step of generating said clock signal further comprises the sub-step of controlling a feedback divider with said sequence of spread spectrum ROM codes.

19. (ORIGINAL) The method according to claim 14, wherein the step of synchronizing said command signal to said

feedback signal further comprises generating one or more control signals in response to (i) said command signal and (ii) said feedback signal.

20. (PREVIOUSLY AMENDED) The method according to claim 19, wherein said one or more control signals are generated by one or more latches configured to sample said command signal in response to said feedback signal.

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21. (PREVIOUSLY RE-PRESENTED, FORMERLY CLAIM 12) An apparatus comprising:

a first circuit configured to generate a clock signal in response to (i) a reference signal, (ii) a sequence of spread spectrum ROM codes, and (iii) a command signal; and

a second circuit configured to synchronize said command signal to a feedback signal, wherein said sequence of spread spectrum ROM codes is generated according to a predetermined mathematical formula and optimized in accordance with predetermined criteria using a computer program to simulate transient behavior of said apparatus.